Claims

1. In a forwarding node for directing data toward a destination, a hardware device comprising:

an input port for receiving data encapsulated in one of multiple formats from a source; and

decapsulation logic for decapsulating the data into a packet format used in the forwarding node without executing processor instructions.

2. The device of claim 1 wherein the device is an application specific integrated circuit (ASIC).

3. The device of claim 1 wherein the device further comprises a programmable pattern storage used by the decapsulation logic for storing information defining what decapsulation is proper for the source.

4. The device of claim 1 wherein the decapsulation logic includes a delineator for delineating Asynchronous Transfer Mode (ATM) cells in the data.

5. The device of claim 4 wherein the delineator locates the ATM cells by looking for a header error control (HEC) field.

6. The device of claim 1 wherein the decapsulation logic includes a Physical Layer Convergence Protocol (PLCP) deframer for deframing PLCP frames.

7. The device of claim 1 wherein the decapsulation logic extracts Internet Protocol (IP) packets from the data.

8. The device of claim 1 wherein the decapsulation logic includes a bit synchronous High Level Data Link Control (HDLC) delineator.

9. The device of claim 1 wherein the decapsulation logic includes an octet synchronous High Level Data Link Control (HDLC) delineator.

10. The device of claim 1 wherein the decapsulation logic includes a Point to Point Protocol (PPP) deframer for deframing PPP frames.

11. The device of claim 1 wherein the decapsulation logic includes a frame relay deframer for deframing frame relay frames.

12. In a forwarding node for directing data toward a destination, a hardware device, comprising:

an output port for outputting data to a destination; and

encapsulation logic for encapsulating the data in a format that is required by the destination using a programmable pattern insertion.

13. The device of claim 12 wherein the device is an application specific integrated circuit (ASIC).

14. The device of claim 12 further comprising a programmable pattern storage used by the encapsulation logic for storing information regarding what encapsulation is proper for the destination.

15. The device of claim 12 wherein the encapsulation logic re-encapsulates the data independent of how the data was originally encapsulated when received by the forwarding node.

16. A forwarding node for directing data from a source toward a destination, comprising:

decapsulation logic for decapsulating the data based on the source; and

encapsulation logic for encapsulating the data based on the destination independent of the source.

17. The forwarding node of claim 16 wherein the decapsulation logic is contained in an application specific integrated circuit (ASIC).

18. The forwarding node of claim 16 wherein the encapsulation logic is contained within an application specific integrated circuit (ASIC).

19. The forwarding node of claim 16 further comprising a programmable pattern storage for use by the decapsulation logic storing information regarding an expected encapsulation of the data.

20. The forwarding node of claim 16 further comprising a programmable storage for use by the encapsulation logic for storing information regarding a proper encapsulation of the data for the destination.

21. The switching node of claim 16 wherein the decapsulation logic includes a frame relay deframer for deframing frame relay frames in the data.

22. The forwarding node of claim 16 wherein the decapsulation logic includes a Point to Point Protocol (PPP) deframer for deframing PPP frames in the data.

23. The forwarding node of claim 16 wherein the encapsulation logic includes a Point to Point Protocol (PPP) framer for encapsulating the data in a PPP frame.

24. The forwarding node of claim 16 wherein the encapsulation logic includes a frame relay framer for encapsulating the data in a frame relay frame.

25. The device of claim 16 wherein the decapsulation logic includes a bit synchronous High Level Data Link Control (HDLC) delineator.

26. The device of claim 16 wherein the decapsulation logic includes an octet synchronous High Level Data Link Control (HDLC) delineator.

27. In a forwarding node having a hardware device for performing decapsulation for directing data from a source to a destination, a method, comprising the steps of:

receiving the data at the forwarding node;

determining the source of the data; and

employing the hardware device to decapsulate the data based on the source of the data.

28. The method of claim 27 wherein the hardware device does not execute computer instructions to decapsulate the data.

29. The method of claim 27 wherein the hardware device extracts Internet Protocol (IP) packets from the data.

30. The method of claim 27 wherein the hardware device extracts Asynchronous Transfer Mode (ATM) cells from the data.

31. The method of claim 27 wherein the hardware uses a pattern matching technique to decapsulate the data.

32. In a forwarding node having a hardware device for encapsulating data, a method comprising the steps of:

providing data to be encapsulated and output from the forwarding node toward a destination.

determining the destination; and

based on the destination, encapsulating the data with the hardware device in a format that is proper for the destination.

33. The method of claim 32 further comprising the step of outputting the data from the forwarding node toward the destination.

34. The method of claim 31 wherein the data is encapsulated to include an adaption layer 5 (AAL5) frame.

35. In a forwarding node for directing data toward a destination, a hardware device, comprising:

an input port for receiving data encapsulated in one of multiple formats from a source; and

decapsulation logic for decapsulating the data into a packet format used in the forwarding node using a pattern matching technique.

36. The device of claim 35 wherein the device is an application specific integrated circuit (ASIC).

37. The device of claim 35 wherein the device further comprises a programmable pattern storage used by the decapsulation logic for storing information defining what decapsulation is proper for the source.

38. The device of claim 35 wherein the decapsulation logic includes a delineator for delineating Asynchronous Transfer Mode (ATM) cells in the data.

39. The device of claim 35 wherein the delineator locates the ATM cells by looking for a header error control (HEC) field.

40. The device of claim 35 wherein the decapsulation logic includes a Physical Layer Convergence Protocol (PLCP) deframer for deframing PLCP frames.

41. The device of claim 35 wherein the decapsulation logic extracts Internet Protocol (IP) packets from the data.

42. The device of claim 35 wherein the decapsulation logic includes a bit synchronous High Level Data Link Control (HDLC) delineator.

43. The device of claim 35 wherein the decapsulation logic includes an octet synchronous High Level Data Link Control (HDLC) delineator.

44. The device of claim 35 wherein the decapsulation logic includes a Point to Point Protocol (PPP) deframer for deframing PPP frames.

45. The device of claim 36 wherein the decapsulation logic includes a frame relay deframer for deframing frame relay frames.